N-Channel Enhancement MOSFET

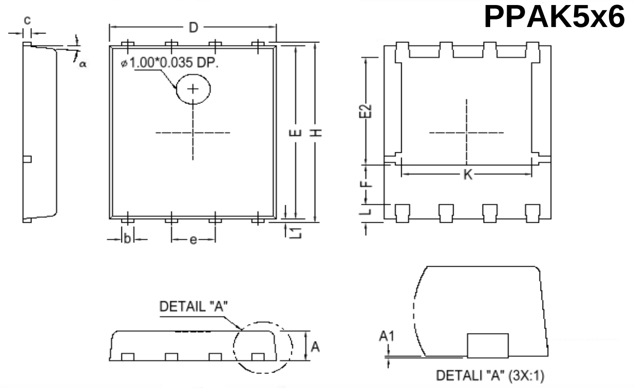
VDS= 30V, ID= 80A

DESCRIPTION

The YS80N03BA is the highest performance N-ch MOSFETs with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications.

The YS80N03BA meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

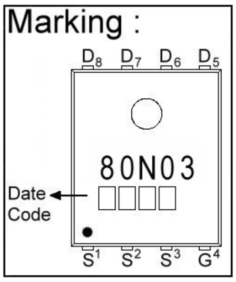
PPAK5x6

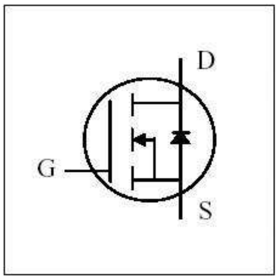


REF.	Millimeter			REF.	Millimeter		
	Min.	Nom.	Max.		Min.	Nom.	Max.
A	0.85	1.00	1.15	E	5.70	-	5.90
A1	0.00	-	0.10	e	-	1.27	-
b	0.30	-	0.51	H	5.90	-	6.20
c	0.20	-	0.30	L	-	0.60	-
D	4.80	-	5.00	L1	0.06	-	0.20
F	1.10REF.			α	0°	-	12°
E2	3.50REF.			K	3.70	3.90	4.10

FEATURES

- Advanced high cell density Trench technology
- Excellent CdV/dt effect decline
- Green Device Available
- Super Low Gate Charge
- 100% EAS Guaranteed





Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current[1]	I_D @T_C=25℃	80	A
	I_D @T_C=100℃	50	A
Pulsed Drain Current[1,2]	I_{DM}	160	A
Total Power Dissipation[4]	P_D @T_C=25℃	53	W
	P_D @T_A=25℃	2	W
Single Pulse Avalanche Energy, L=0.1mH[3]	E_{AS}	88	mJ
Single Pulse Avalanche Current, L=0.1mH[3]	I_{AS}	42	A
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 ~ +150	℃

Thermal Data

Parameter	Symbol	Conditions	Max. Value	Unit
Thermal Resistance Junction-ambient[1]	$R_{\theta JA}$	Steady State	62.5	℃/W
Thermal Resistance Junction-case[1]	$R_{\theta JC}$	Steady State	2.36	℃/W

DEVICE CHARACTERISTICS

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Electrical Characteristics (T_J = 25℃ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV_{DSS}	30	-	-	V	V_{GS}=0, I_D=250uA
Gate Threshold Voltage	$V_{GS(th)}$	1.0	-	2.5	V	V_{DS}=V_{GS}, I_D=250uA
Forward Transconductance	g_{fs}	-	18	-	S	V_{DS}=10V, I_D=10A
Gate-Source Leakage Current	I_{GSS}	-	-	±100	nA	V_{GS}= ±20V
Drain-Source Leakage Current(T_J=25℃)	I_{DSS}	-	-	1	uA	V_{DS}=30V, V_{GS}=0
Drain-Source Leakage Current(T_J=125℃)		-	-	10		V_{DS}=24V, V_{GS}=0
Static Drain-Source On-Resistance[2]	$R_{DS(ON)}$	-	-	5.5	mΩ	V_{GS}=10V, I_D=20A
		-	-	8		V_{GS}=4.5V, I_D=10A
Total Gate Charge[2]	Q_g	-	11.1	-	nC	I_D=20A V_{DS}=15V V_{GS}=4.5V
Gate-Source Charge	Q_{gs}	-	1.9	-		
Gate-Drain (“Miller”) Change	Q_{gd}	-	6.8	-		
Turn-on Delay Time[2]	$T_{d(on)}$	-	7.5	-	ns	V_{DD}=15V I_D=15A V_{GS}=10V R_G=3.3Ω
Rise Time	T_r	-	14.5	-		
Turn-off Delay Time	$T_{d(off)}$	-	35.2	-		
Fall Time	T_f	-	9.6	-		
Input Capacitance	C_{iss}	-	1160	-	pF	V_{GS}=0V V_{DS}=25V f=1.0MHz
Output Capacitance	C_{oss}	-	200	-		
Reverse Transfer Capacitance	C_{rss}	-	180	-		
Gate Resistance	R_g	-	2.5	3.5	Ω	f=1.0MHz

Guaranteed Avalanche Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Single Pulse Avalanche Energy[5]	EAS	20	-	-	mJ	V_{DD}=25V, L=0.1mH, I_{AS}=20A

Source-Drain Diode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Diode Forward Voltage[2]	V_{SD}	-	-	1.2	V	I_S=20A, V_{GS}=0V, T_J=25℃
Continuous Source Current[1,6]	I_S	-	-	80	A	V_G=V_D=0V, Force Current
Pulsed Source Current[2,6]	I_{SM}	-	-	160	A	

Notes: **1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.**

2. The data tested by pulsed, pulse width ≦ 300us, duty cycle ≦ 2%.

3. The EAS data shows Max. rating. The test condition is VDD=25V, VGS=10V, L=0.1mH, IAS=42A.

4. The power dissipation is limited by 150℃ junction temperature.

5. The Min. value is 100% EAS tested guarantee.

6. The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation.

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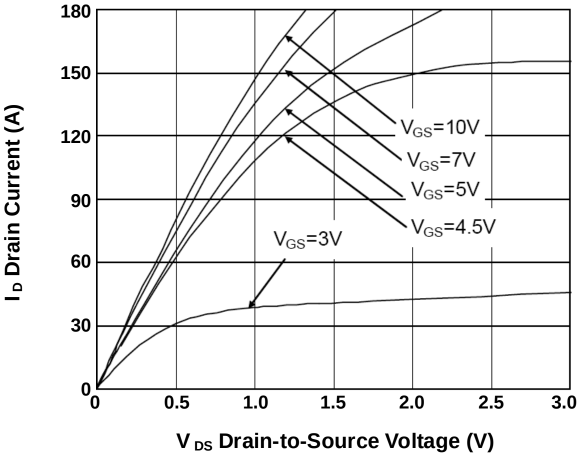

Fig.1 Typical Output Characteristics

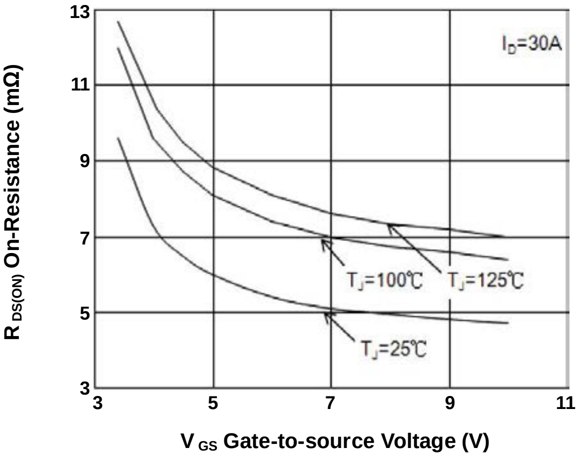

Fig.2 On-Resistance vs. G-S Voltage

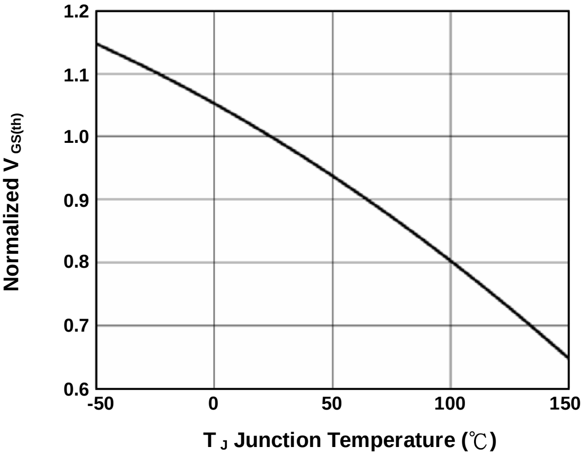

Fig.3 Normalized $V_{GS(th)}$ vs. T_J

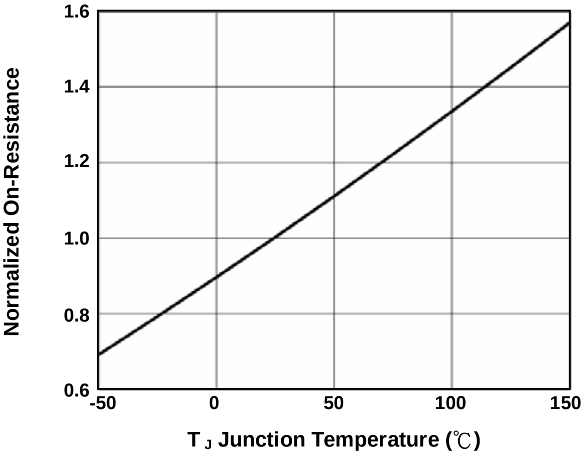

Fig.4 Normalized R_{DSON} vs. T_J

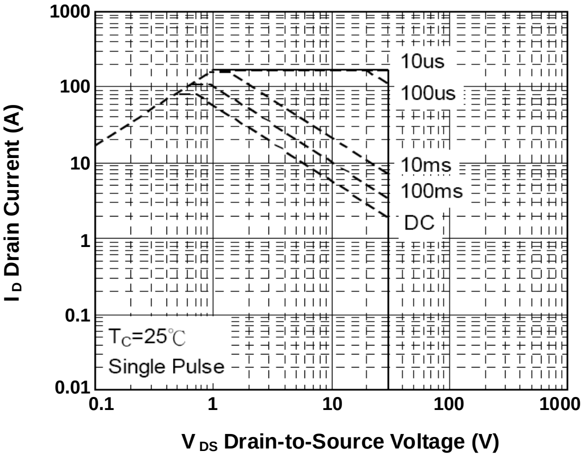

Fig.5 Safe Operating Area

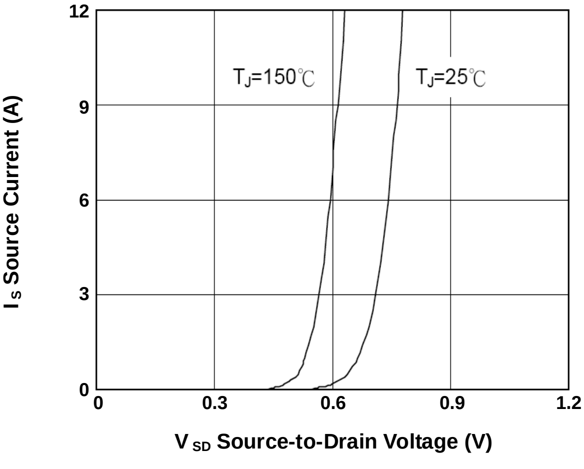

Fig.6 Forward Characteristics of Reverse

DEVICE CHARACTERISTICS

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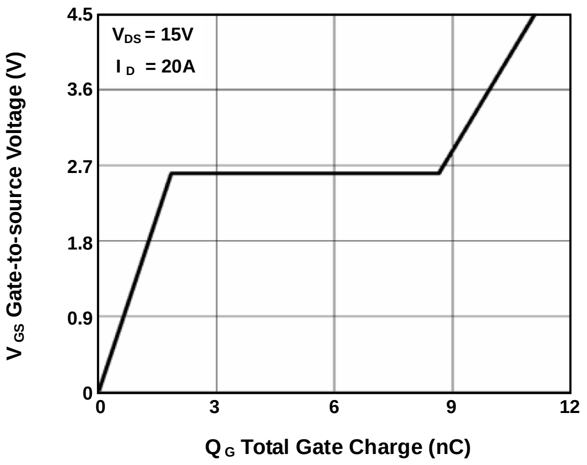

Fig.7 Gate Charge Characteristics

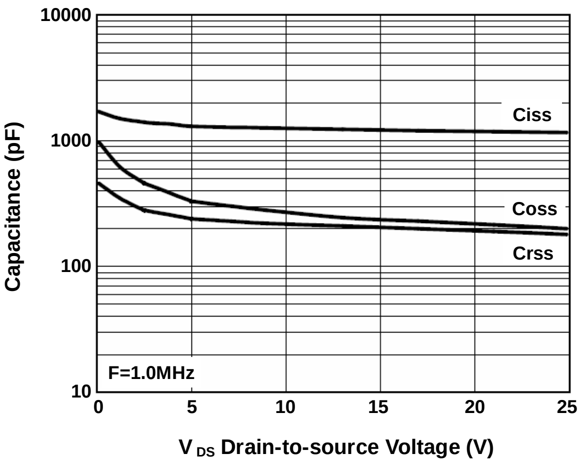

Fig.8 Capacitance Characteristics

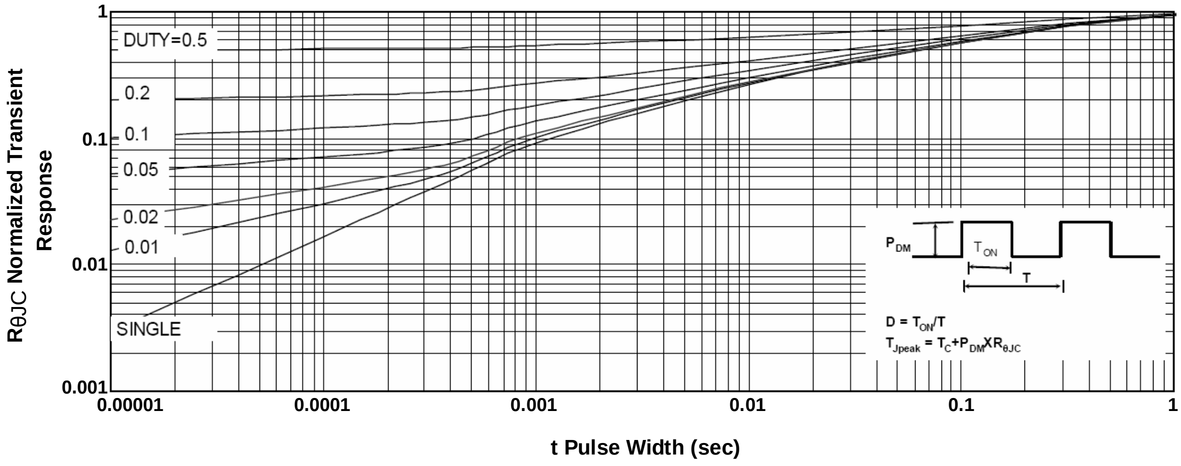

Fig.9 Normalized Maximum Transient Thermal Impedance

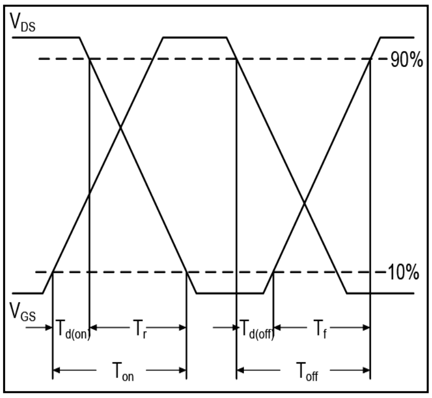

Fig.10 Switching Time Waveform

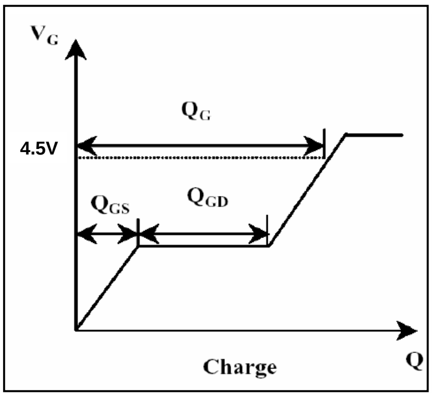

Fig.11 Gate Charge Waveform