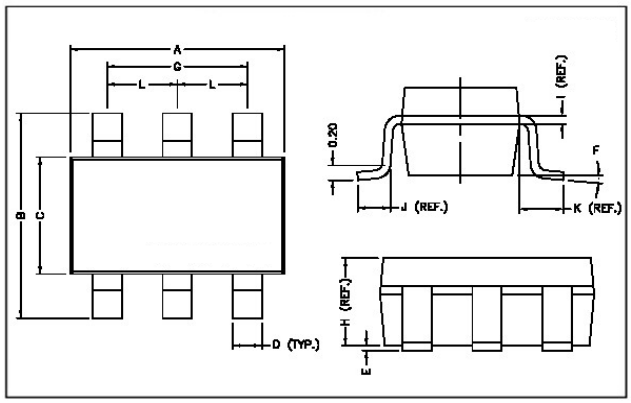
YEA SHIN TECHNOLOGY CO., LTD

YS6604SQ

N+P-Channel Enhancement MOSFET

N-ch: VDS= 20V, ID= 3.6A / P-ch: VDS= -20V, ID= -3.0A

SOT-26



DESCRIPTION

The YS6604SQ uses advanced trench technology to provide excellent on-resistance and low gate change. The complementary MOSFETs form a high-speed power inverter, suitable for a multitude of applications.

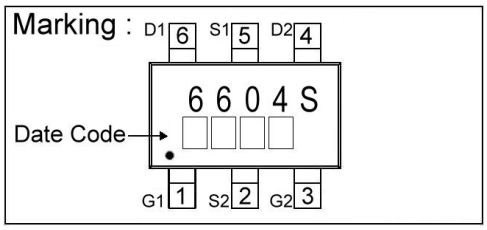
The SOT-26 package is universally used for all commercial-industrial surface mount applications.

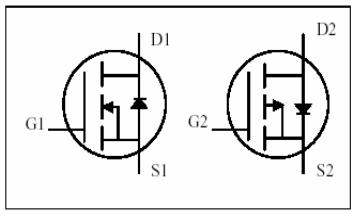
FEATURES

- Low Gate Charge
- Low On-resistance
- Green Device Available

REF.	Millimeter		REF.	Dimensions
	Min.	Max.		Millimeter
A	2.70	3.10	G	1.90 REF.
B	2.60	3.00	H	1.20 REF.
C	1.40	1.80	I	0.12 REF.
D	0.30	0.50	J	0.37 REF.
E	0	0.10	K	0.60 REF.
F	0°	10°	L	0.95 REF.

MARKING





Absolute Maximum Ratings

Parameter	Symbol	Ratings		Unit
		N-channel	P-channel	
Drain-Source Voltage	V_{DS}	20	-20	V
Gate-Source Voltage	V_{GS}	± 10	± 10	V
Continuous Drain Current[1] V_{GS}@4.5V	I_D @T_A=25℃	3.6	-3.0	A
Continuous Drain Current[1] V_{GS}@4.5V	I_D @T_A=70℃	2.8	-2.4	A
Pulsed Drain Current[2]	I_{DM}	14.4	-13.2	A
Total Power Dissipation[3]	P_D @T_A=25℃	1.1		W
Operating Junction and Storage Temperature Range	Tj, Tstg	-55 ~ +150		℃

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance Junction-ambient[1] Max.	$R_{\theta JA}$	110	℃/W

DEVICE CHARACTERISTICS

YS6604SQ

N-Channel Electrical Characteristics (Tj = 25℃ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV_{DSS}	20	-	-	V	V_{GS}=0, I_D=250uA
Gate Threshold Voltage	$V_{GS(th)}$	0.4	-	1.0	V	V_{DS}=V_{GS}, I_D=250uA
Forward Transconductance	g_{fs}	-	10	-	S	V_{DS}=5V, I_D=3A
Gate-Source Leakage Current	I_{GSS}	-	-	±100	nA	V_{GS}= ±10V
Drain-Source Leakage Current(Tj=25℃)	I_{DSS}	-	-	1	uA	V_{DS}=16V, V_{GS}=0
Drain-Source Leakage Current(Tj=55℃)		-	-	5	uA	V_{DS}=16V, V_{GS}=0
Static Drain-Source On-Resistance[2]	$R_{DS(ON)}$	-	-	48	mΩ	V_{GS}=4.5V, I_D=3A
		-	-	55		V_{GS}=2.5V, I_D=2A
		-	-	95		V_{GS}=1.8V, I_D=1A
Total Gate Charge[2]	Q_g	-	4.6	-	nC	I_D=3A V_{DS}=15V V_{GS}=4.5V
Gate-Source Charge	Q_{gs}	-	0.7	-		
Gate-Drain (“Miller”) Change	Q_{gd}	-	1.5	-		
Turn-on Delay Time[2]	$T_{d(on)}$	-	1.6	3.2	ns	V_{DS}=10V I_D=3A V_{GS}=4.5V R_G=3.3Ω
Rise Time	T_r	-	42	84		
Turn-off Delay Time	$T_{d(off)}$	-	14	28		
Fall Time	T_f	-	7	14		
Input Capacitance	C_{iss}	-	310	434	pF	V_{GS}=0V V_{DS}=15V f=1.0MHz
Output Capacitance	C_{oss}	-	49	-		
Reverse Transfer Capacitance	C_{rss}	-	35	-		

Source-Drain Diode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Diode Forward Voltage[2]	V_{SD}	-	-	1.2	V	I_S=1A, V_{GS}=0V, T_J=25℃
Continuous Source Current[1,4]	I_S	-	-	3.6	A	V_G=V_D=0V, Force Current

Notes: 1. Surface mounted on 1 in^2 copper pad of FR4 board, t≦5sec; 180℃/W when mounted on Min. copper pad.

2. The data tested by pulsed, pulse width ≦ 300us, duty cycle ≦ 2%.

3. The power dissipation is limited by 150℃ junction temperature.

4. The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation.

DEVICE CHARACTERISTICS

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P-Channel Electrical Characteristics (Tj = 25℃ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV_{DSS}	-20	-	-	V	V_{GS}=0, I_D=-250uA
Gate Threshold Voltage	$V_{GS(th)}$	-0.4	-	-1.0	V	V_{DS}=V_{GS}, I_D=-250uA
Forward Transconductance	g_{fs}	-	7	-	S	V_{DS}=-5V, I_D=-2.8A
Gate-Source Leakage Current	I_{GSS}	-	-	±100	nA	V_{GS}= ±10V
Drain-Source Leakage Current(Tj=25℃)	I_{DSS}	-	-	-1	uA	V_{DS}=-16V, V_{GS}=0
Drain-Source Leakage Current(Tj=55℃)		-	-	-5	uA	V_{DS}=-16V, V_{GS}=0
Static Drain-Source On-Resistance[2]	$R_{DS(ON)}$	-	-	80	mΩ	V_{GS}=-4.5V, I_D=-3A
		-	-	120		V_{GS}=-2.5V, I_D=-2A
		-	-	160		V_{GS}=-1.8V, I_D=-1A
Total Gate Charge	Q_g	-	4.8	-	nC	I_D=-3A V_{DS}=-10V V_{GS}=-4.5V
Gate-Source Charge	Q_{gs}	-	0.5	-		
Gate-Drain (“Miller”) Change	Q_{gd}	-	2.1	-		
Turn-on Delay Time[2]	$T_{d(on)}$	-	3.6	7	ns	V_{DS}=-10V I_D=-1A V_{GS}=-4.5V R_G=25Ω
Rise Time	T_r	-	12.5	25		
Turn-off Delay Time	$T_{d(off)}$	-	32.5	65		
Fall Time	T_f	-	8.5	17		
Input Capacitance	C_{iss}	-	350	515	pF	V_{GS}=0V V_{DS}=-15V f=1.0MHz
Output Capacitance	C_{oss}	-	66	-		
Reverse Transfer Capacitance	C_{rss}	-	50	-		

Source-Drain Diode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Forward On Voltage[2]	V_{SD}	-	-	-1.0	V	I_S=-1.0A, V_{GS}=0V
Continuous Source Current[1,4]	I_S	-	-	-3.0	A	V_G=V_D=0V, Force Current

Notes: 1. Surface mounted on 1 in^2 copper pad of FR4 board, t≦5sec; 180℃/W when mounted on Min. copper pad.

2. The data tested by pulsed, pulse width ≦ 300us, duty cycle ≦ 2%.

3. The power dissipation is limited by 150℃ junction temperature.

4. The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation.

DEVICE CHARACTERISTICS

YS6604SQ

Typical Characteristics N-Channel

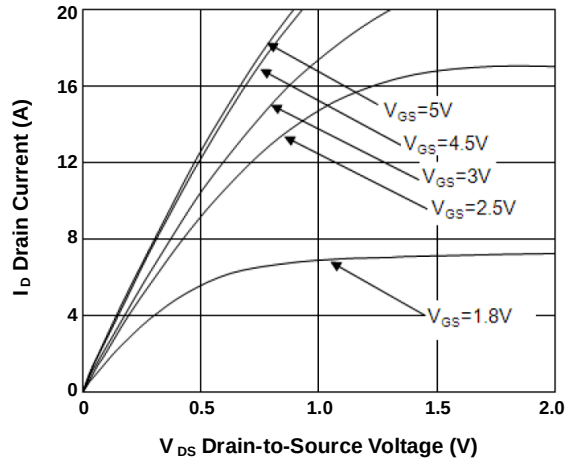

Fig.1 Typical Output Characteristics

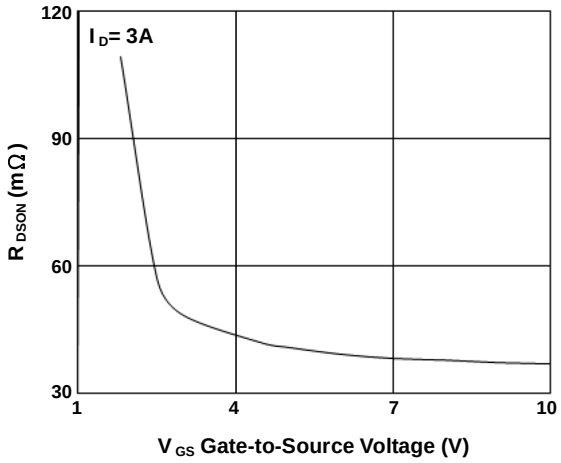

Fig.2 On-Resistance vs. G-S Voltage

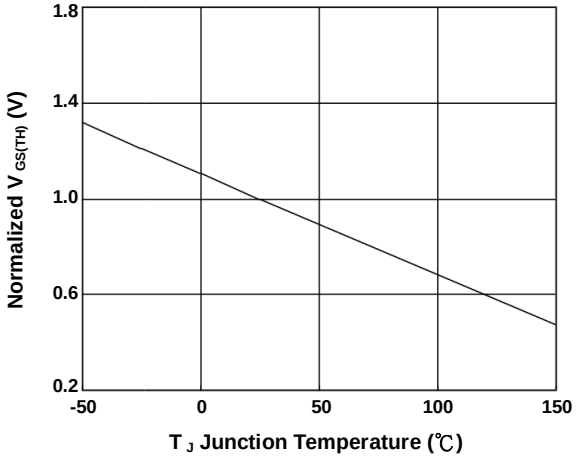

Fig.3 Normalized $V_{GS(th)}$ vs. T_J

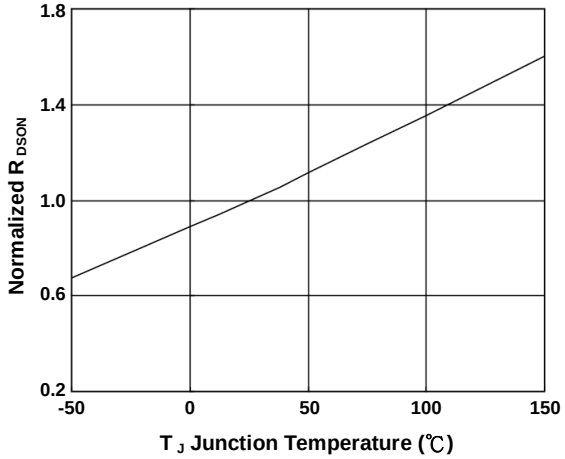

Fig.4 Normalized R_{DSON} vs. T_J

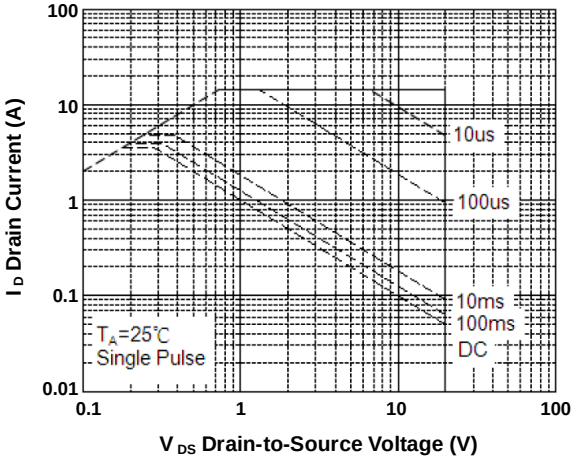

Fig.5 Safe Operating Area

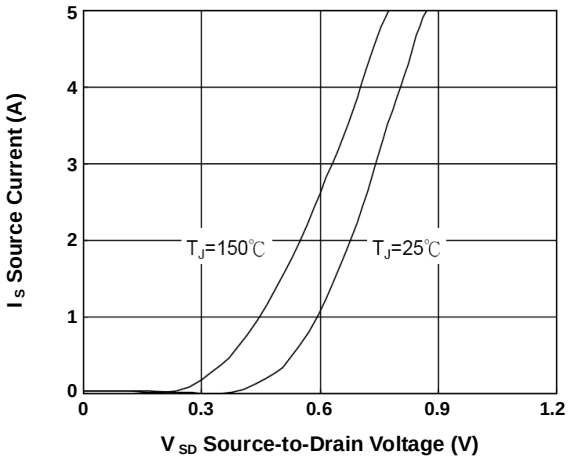

Fig.6 Forward Characteristics of Reverse

DEVICE CHARACTERISTICS

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Typical Characteristics N-Channel

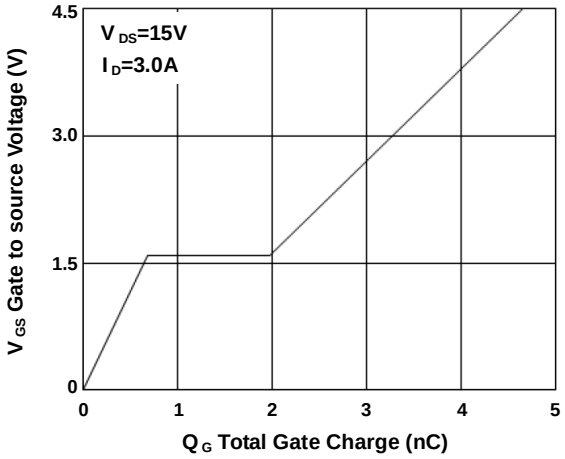

Fig.7 Gate Charge Characteristics

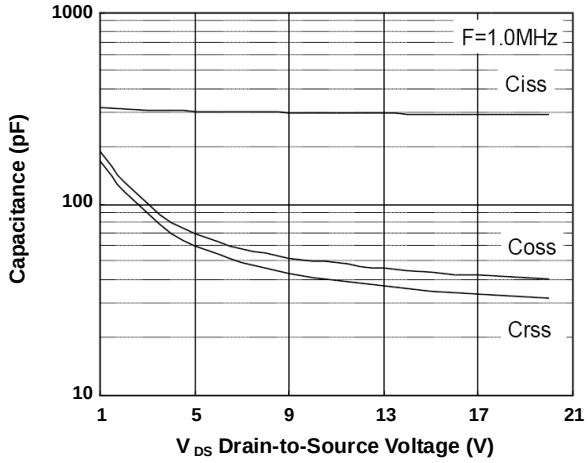

Fig.8 Capacitance Characteristics

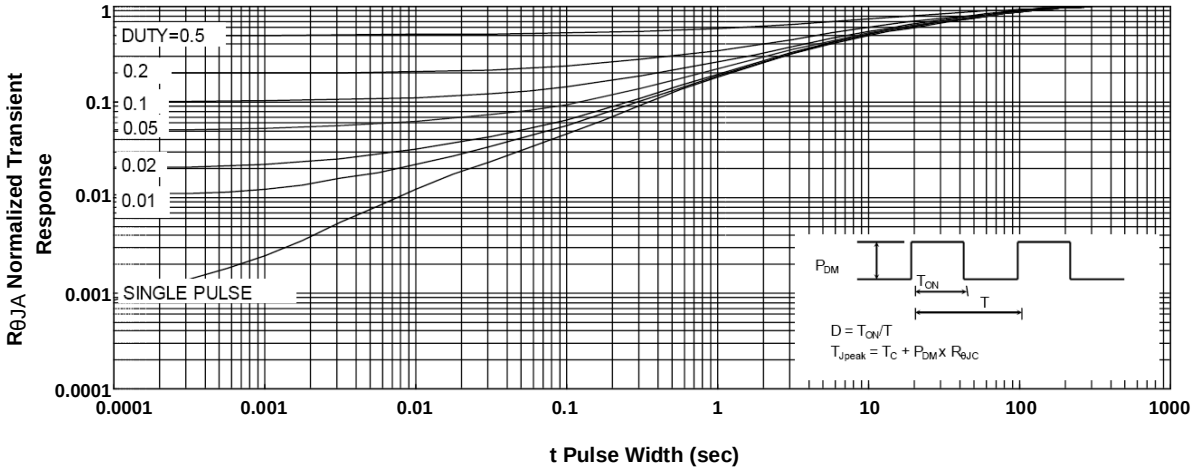

Fig.9 Normalized Maximum Transient Thermal Impedance

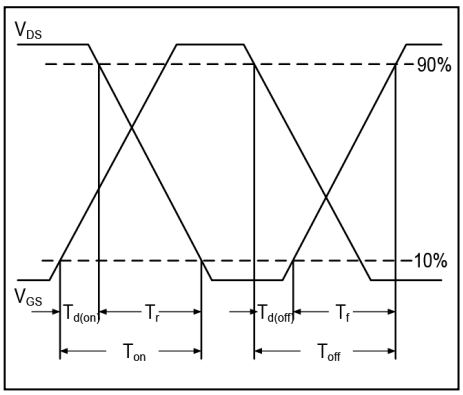

Fig.10 Switching Time Waveform

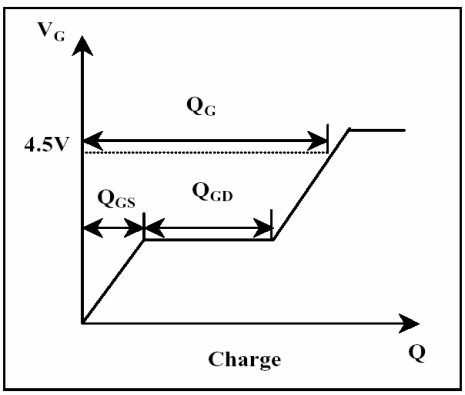

Fig.11 Gate Charge Waveform

DEVICE CHARACTERISTICS

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Typical Characteristics P-Channel

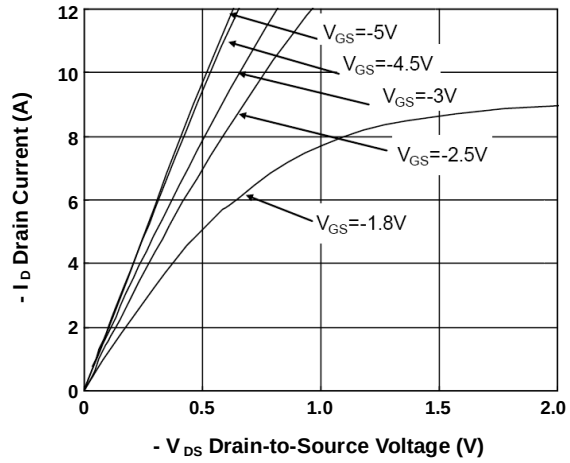
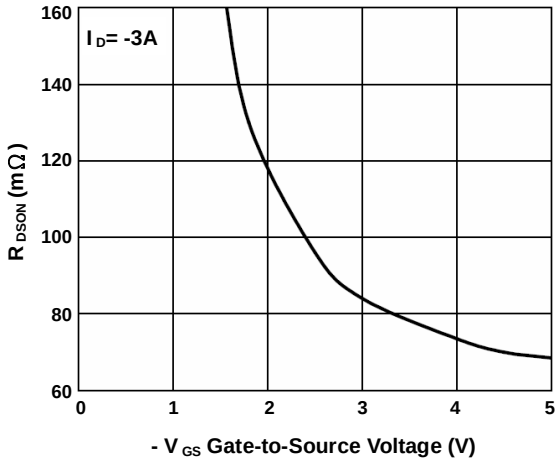


Fig.1 Typical Output Characteristics



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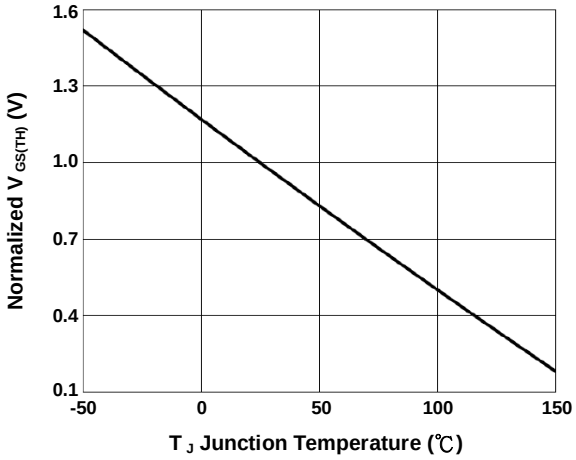

Fig.3 Normalized $V_{GS(th)}$ vs. T_J

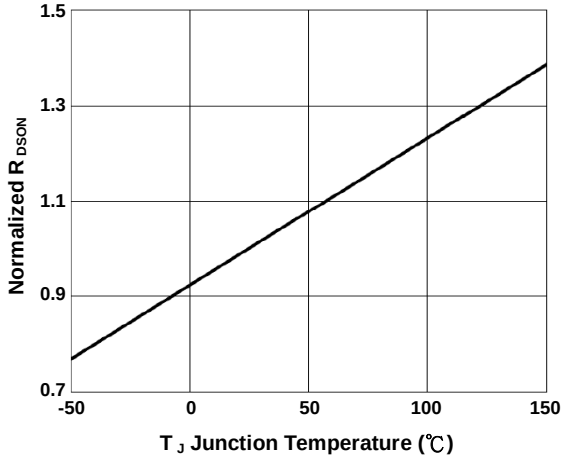

Fig.4 Normalized R_{DSON} vs. T_J

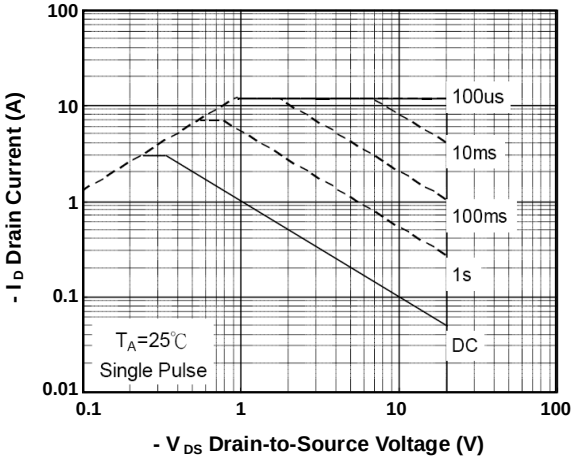

Fig.5 Safe Operating Area

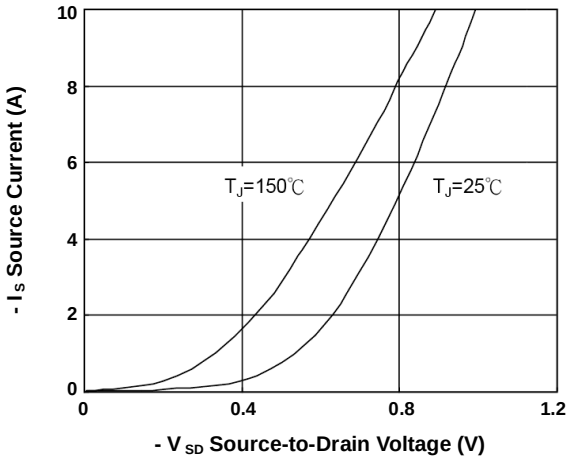

Fig.6 Forward Characteristics of Reverse

DEVICE CHARACTERISTICS

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Typical Characteristics P-Channel

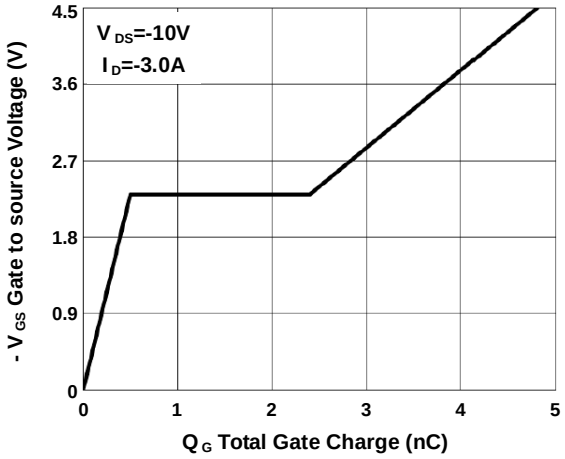


Fig.7 Gate Charge Characteristics

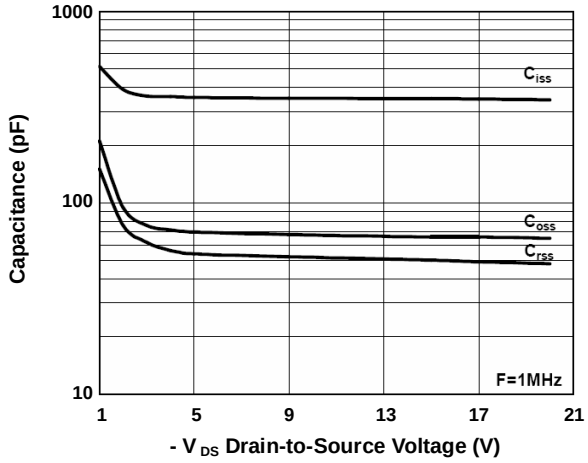
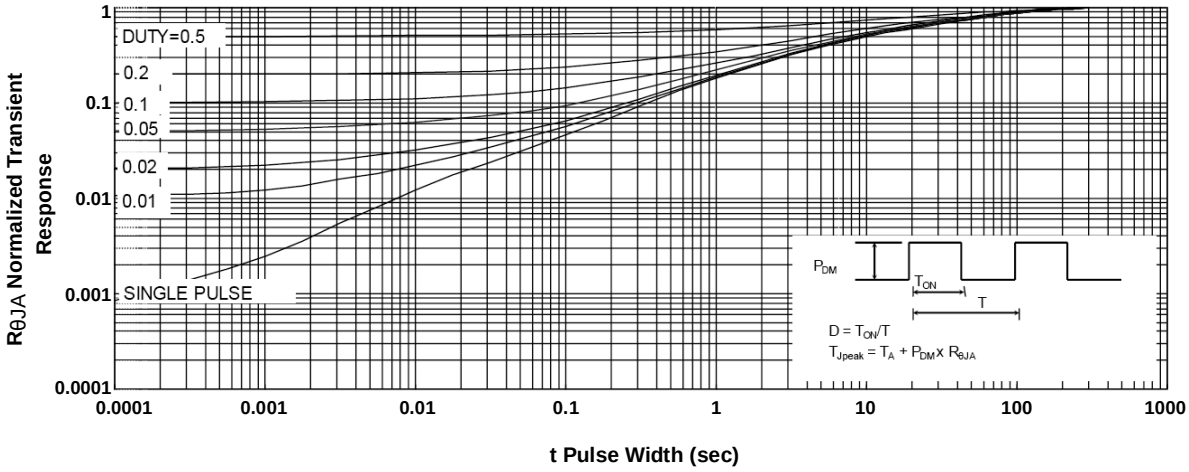


Fig.8 Capacitance Characteristics



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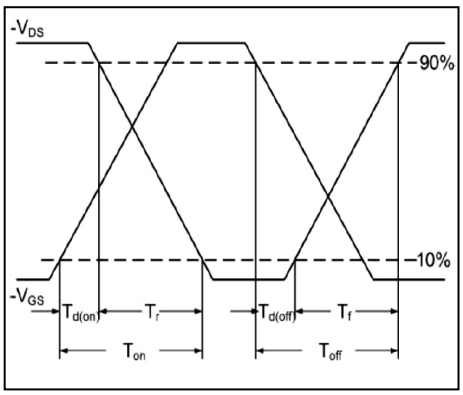

Fig.10 Switching Time Waveform

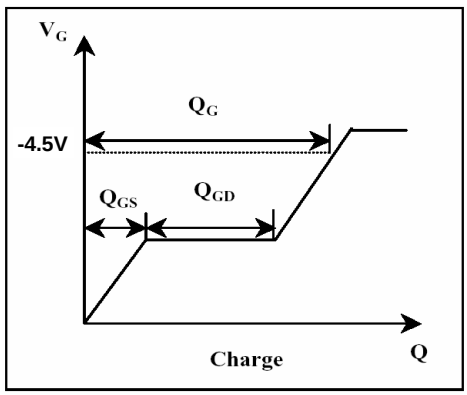

Fig.11 Gate Charge Waveform