

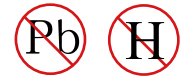


YEA SHIN TECHNOLOGY CO., LTD

YS60N04AP

N-Channel Enhancement MOSFET

VDS= 60V, ID= 55A



Description

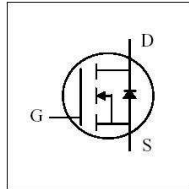
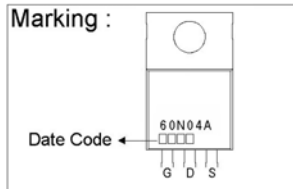
The YS60N04AP is using trench DMOS technology. This advanced technology has been especially tailored to minimize $R_{DS(ON)}$, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

The YS60N04AP meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

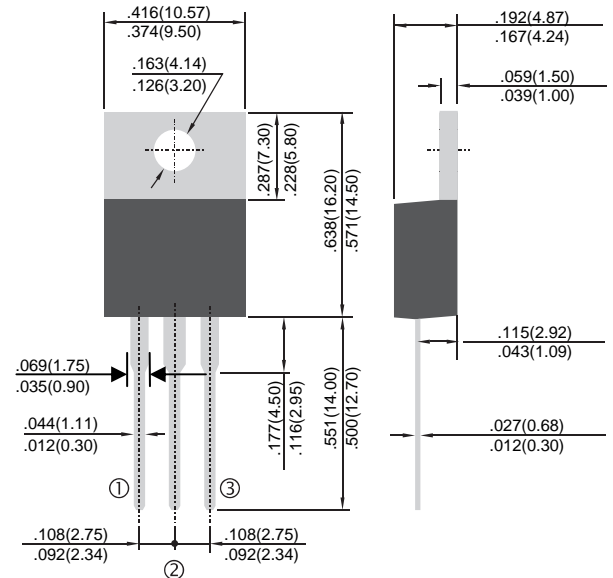
Feature

- Low On-Resistance
- Improve dv/dt Capability
- Green Device Available
- Fast switching
- 100% EAS Guaranteed

Marking :



TO-220 Unit:inch(mm)



Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ¹	$I_D @ T_C=25^\circ C$	55	A
	$I_D @ T_C=100^\circ C$	35	A
Pulsed Drain Current ^{1,2}	I_{DM}	220	A
Total Power Dissipation ⁴	$P_D @ T_C=25^\circ C$	96	W
	$P_D @ T_A=25^\circ C$	2	W
Single Pulse Avalanche Energy, $L=0.1mH^3$	E_{AS}	61	mJ
Single Pulse Avalanche Current, $L=0.1mH^3$	I_{AS}	35	A
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 ~ +150	$^\circ C$

Thermal Data

Parameter	Symbol	Conditions	Max. Value	Unit
Thermal Resistance Junction-ambient ¹	$R_{\theta JA}$	Steady State	62.5	$^\circ C/W$
Thermal Resistance Junction-case ¹	$R_{\theta JC}$	Steady State	1.3	$^\circ C/W$

DEVICE CHARACTERISTICS

YS60N04AP

Electrical Characteristics (T_j = 25°C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV _{DSS}	60	-	-	V	V _{GS} =0, I _D =250uA
Gate Threshold Voltage	V _{GS(th)}	1.2	1.6	2.5	V	V _{DS} =V _{GS} , I _D =250uA
Forward Transconductance	g _{fs}	-	11.5	-	S	V _{DS} =10V, I _D =6A
Gate-Source Leakage Current	I _{GSS}	-	-	±100	nA	V _{GS} = ±20V
Drain-Source Leakage Current(T _j =25°C)	I _{DSS}	-	-	1	uA	V _{DS} =60V, V _{GS} =0
Drain-Source Leakage Current(T _j =125°C)		-	-	10	uA	V _{DS} =48V, V _{GS} =0
Static Drain-Source On-Resistance	R _{DS(ON)}	-	10.5	12	mΩ	V _{GS} =10V, I _D =30A
		-	12	15		V _{GS} =4.5V, I _D =15A
Total Gate Charge ²	Q _g	-	39.2	-	nC	I _D =10A V _{DS} =30V V _{GS} =10V
Gate-Source Charge	Q _{gs}	-	5.9	-		
Gate-Drain ("Miller") Change	Q _{gd}	-	8.8	-		
Turn-on Delay Time ²	T _{d(on)}	-	9.6	-	ns	V _{DS} =15V I _D =1A V _{GS} =10V R _G =6Ω
Rise Time	T _r	-	28.2	-		
Turn-off Delay Time	T _{d(off)}	-	45.3	-		
Fall Time	T _f	-	10.9	-		
Input Capacitance	C _{iss}	-	2100	-	pF	V _{GS} =0V V _{DS} =25V f=1.0MHz
Output Capacitance	C _{oss}	-	165	-		
Reverse Transfer Capacitance	C _{rss}	-	80	-		
Gate Resistance	R _g	-	1.6	3.2	Ω	f=1.0MHz

Guaranteed Avalanche Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Single Pulse Avalanche Energy ⁵	EAS	33.8	-	-	mJ	V _{DD} =25V, L=0.1mH, I _{AS} =26A

Source-Drain Diode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Diode Forward Voltage ²	V _{SD}	-	-	1.2	V	I _S =30A, V _{GS} =0V, T _J =25°C
Continuous Source Current ^{1,6}	I _S	-	-	55	A	V _G =V _D =0V, Force Current
Pulsed Source Current ^{2,6}	I _{SM}	-	-	220	A	

Notes: 1. The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.

2. The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%.

3. The EAS data shows Max. rating. The test condition is V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=35A.

4. The power dissipation is limited by 150°C junction temperature.

5. The Min. value is 100% EAS tested guarantee.

6. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

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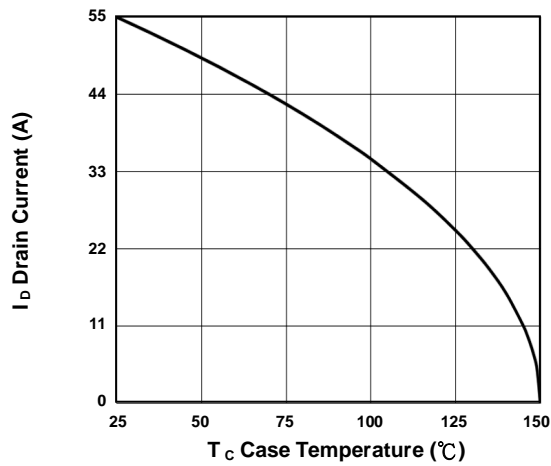


Fig.1 Drain Current vs. T_C

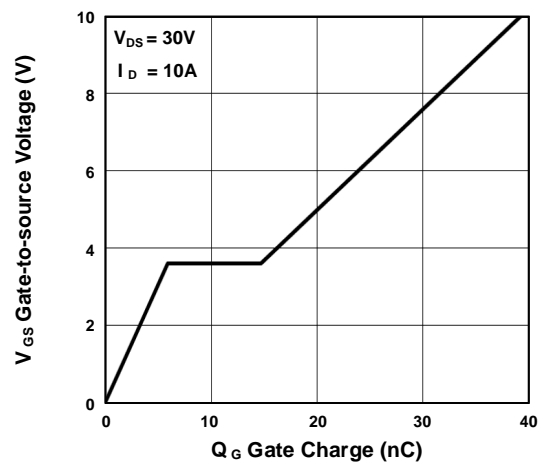


Fig.2 Gate Charge Characteristics

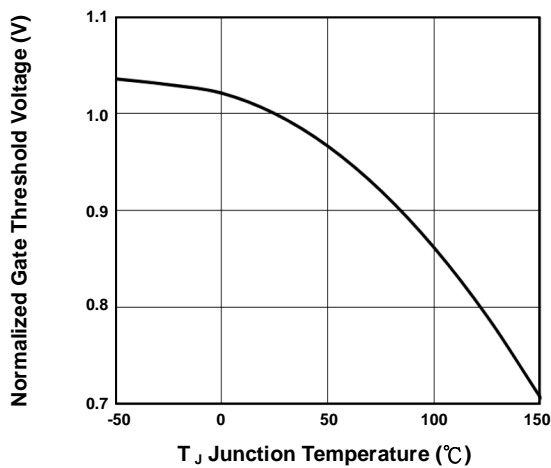


Fig.3 Normalized $V_{GS(th)}$ vs. T_J

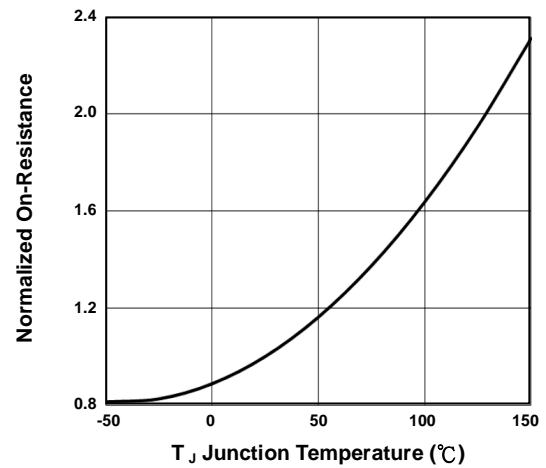


Fig.4 Normalized $R_{DS(on)}$ vs. T_J

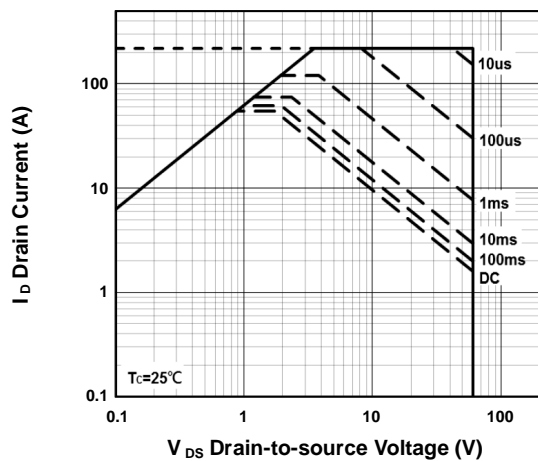


Fig.5 Safe Operating Area

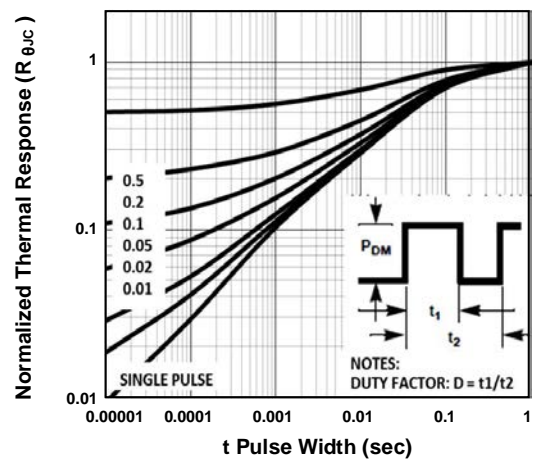


Fig.6 Transient Thermal Impedance

DEVICE CHARACTERISTICS

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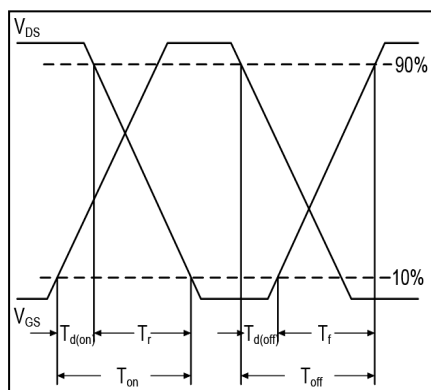


Fig.7 Switching Time Waveform

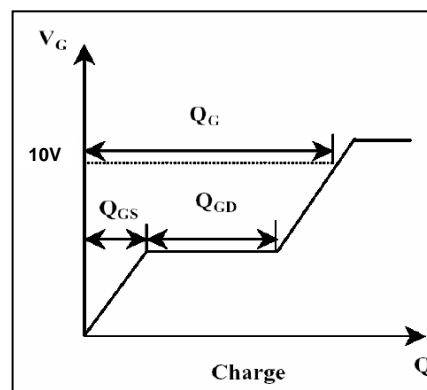


Fig.8 Gate Charge Waveform