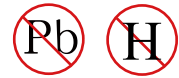


**N-Channel Enhancement MOSFET****V_{DS}= 100V, I_D= 15A****DESCRIPTION**

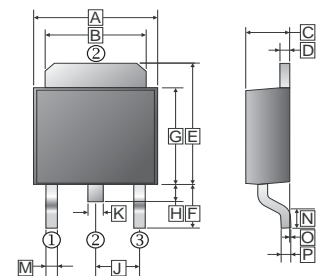
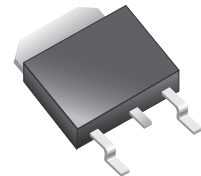
combination of fast switching. The TO-252 package is universally preferred for all commercial-industrial surface mount applications. The device is suited for charger, industrial and consumer environment.

FEATURES

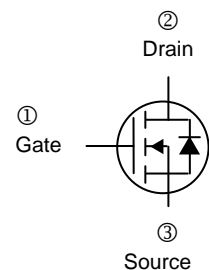
- $R_{DS(on)} \leq 100m\Omega$ @ $V_{GS} = 10V$
- Super high density cell design for extremely low $R_{DS(on)}$
- Exceptional on-resistance and maximum DC current capability

MARKING**PACKAGE INFORMATION**

Package	MPQ	Leader Size
TO-252	2.5K	13' inch

TO-252(D-PAK)

REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	6.4	6.8	J	2.30 REF.	
B	5.20	5.50	K	0.70	0.90
C	2.20	2.40	M	0.50	1.1
D	0.45	0.58	N	0.9	1.6
E	6.8	7.3	O	0	0.15
F	2.40	3.0	P	0.43	0.58
G	5.40	6.2			
H	0.8	1.20			

**ABSOLUTE MAXIMUM RATINGS** ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	$T_C=25^\circ\text{C}$	15
		$T_C=70^\circ\text{C}$	13.8
Pulsed Drain Current ¹	I_{DM}	24	A
Power Dissipation	P_D	$T_C=25^\circ\text{C}$	44.6
		$T_A=25^\circ\text{C}$	2
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 ~ 150	$^\circ\text{C}$
Thermal Resistance Ratings			
Maximum Thermal Resistance Junction-Ambient (PCB mount) ³	$R_{\theta JA}$	62.5	$^\circ\text{C} / \text{W}$
Maximum Thermal Resistance Junction-Case	$R_{\theta JC}$	2.8	$^\circ\text{C} / \text{W}$

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
Drain-Source Breakdown Voltage	BV _{DSS}	100	-	-	V	V _{GS} =0, I _D =250μA
Gate Threshold Voltage	V _{GS(th)}	1.0	-	2.5	V	V _{DS} =V _{GS} , I _D =250μA
Gate-Source Leakage Current	I _{GSS}	-	-	±100	nA	V _{GS} = ±20V
Drain-Source Leakage Current	I _{DSS}	-	-	1	μA	V _{DS} =80V, V _{GS} =0
Static Drain-Source On-Resistance ²	R _{DS(on)}	-	100	110	mΩ	V _{GS} =10V, I _D =8A
Total Gate Charge ²	Q _g	-	26.2	-	nC	I _D =10A V _{DS} =80V V _{GS} =10V
Gate-Source Charge	Q _{gs}	-	4.6	-		
Gate-Drain ("Miller") Charge	Q _{gd}	-	5.1	-		
Turn-on Delay Time ²	T _{d(on)}	-	4.2	-	nS	V _{DS} =50V I _D = 10A V _{GS} =10V R _L =5Ω R _G =3.3Ω
Rise Time	T _r	-	8.2	-		
Turn-off Delay Time	T _{d(off)}	-	35.6	-		
Fall Time	T _f	-	9.6	-		
Input Capacitance	C _{iss}	-	1535	-	pF	V _{GS} =0 V _{DS} =15V f=1.0MHz
Output Capacitance	C _{oss}	-	60	-		
Reverse Transfer Capacitance	C _{rss}	-	37	-		
Gate Resistance	R _g	-	2	-	Ω	f=1.0MHz
Source-Drain Diode						
Forward On Voltage ²	V _{SD}	-	-	1.2	V	I _S =8.0A, V _{GS} =0V

Notes:

1. Pulse width limited by maximum junction temperature.
2. Pulse test.
3. Surface Mounted on 1 in₂ copper pad of FR4 Board.

DEVICE CHARACTERISTICS

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CHARACTERISTICS CURVE

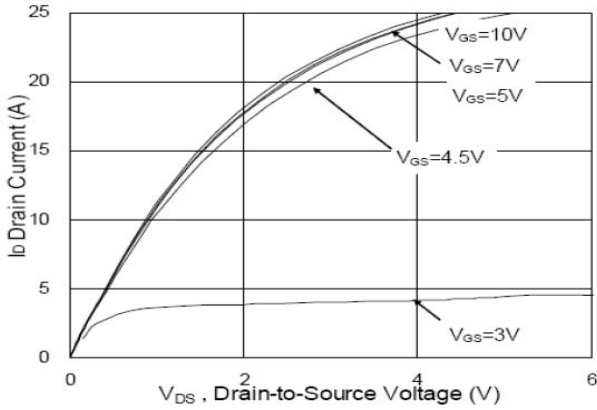


Fig 1. Typical Output Characteristics

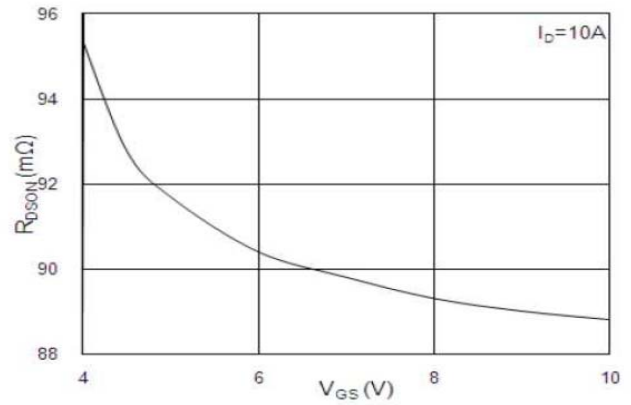


Fig 2. On-Resistance vs. Gate-Source

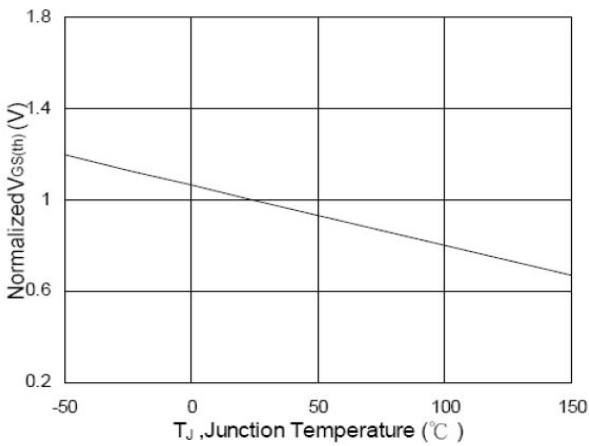


Fig 3. Gate Threshold Voltage vs. Junction Temperature

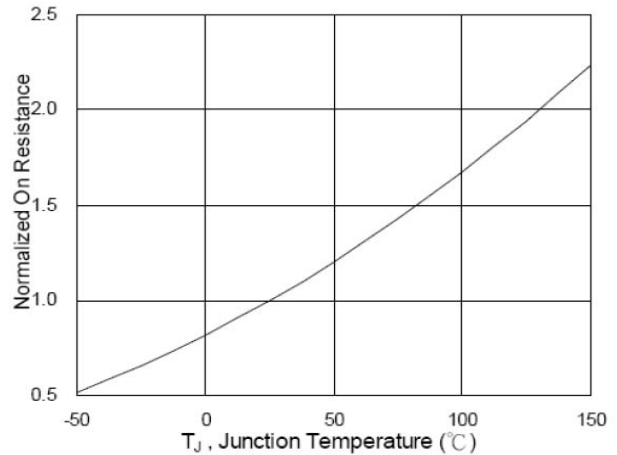


Fig 4. On-Resistance vs. Junction Temperature

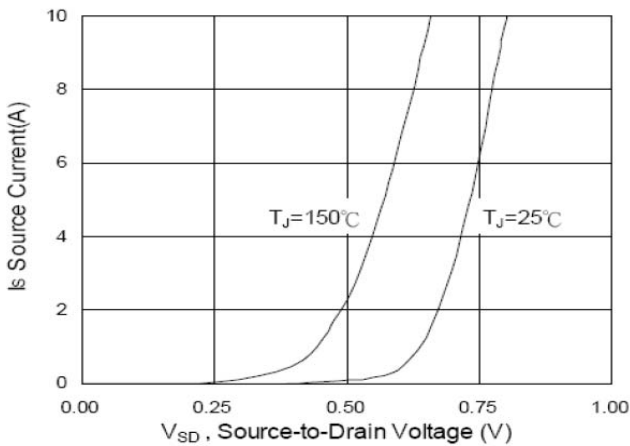


Fig 5. Forward Characteristics of Reverse Diode

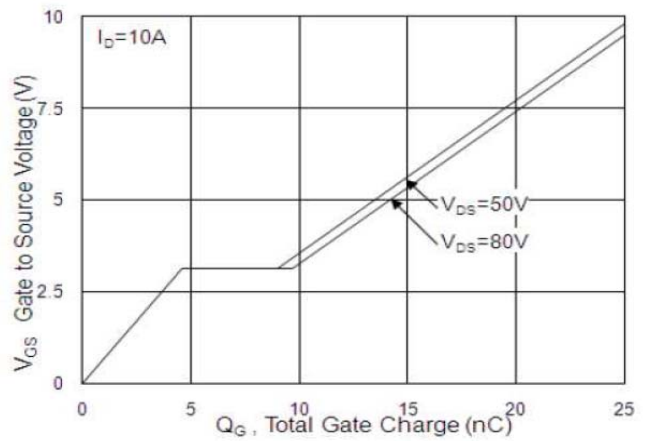


Fig 6. Gate Charge Characteristics

DEVICE CHARACTERISTICS

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CHARACTERISTICS CURVE

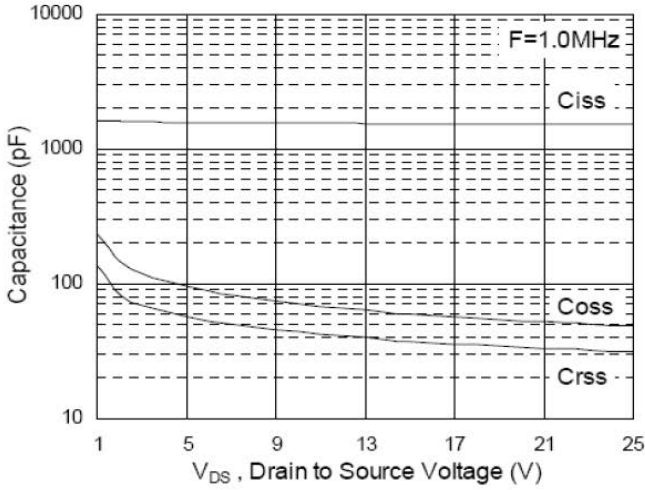


Fig 7. Typical Capacitance Characteristics

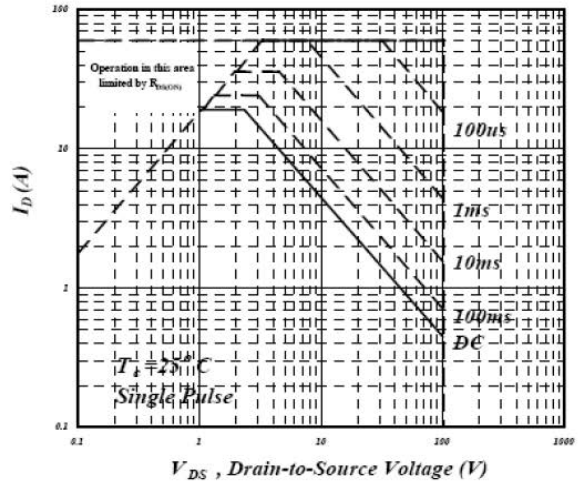


Fig 8. Maximum Safe Operating Area

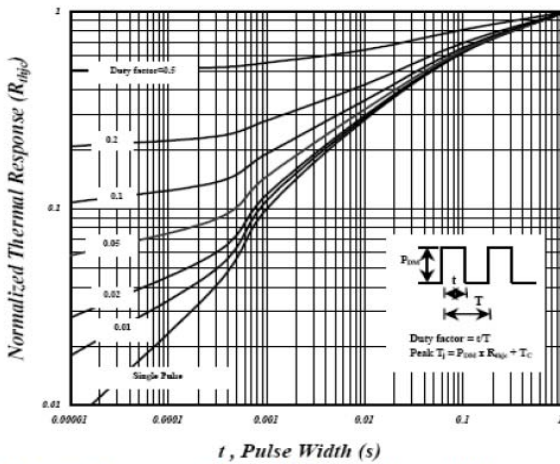


Fig 9. Normalized Transient Thermal Resistance vs. Pulse Width

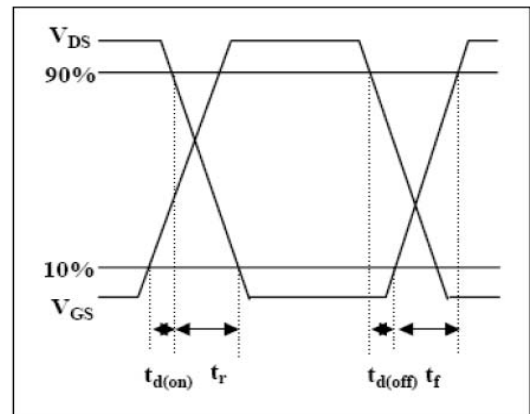


Fig 10. Switching Time Waveform

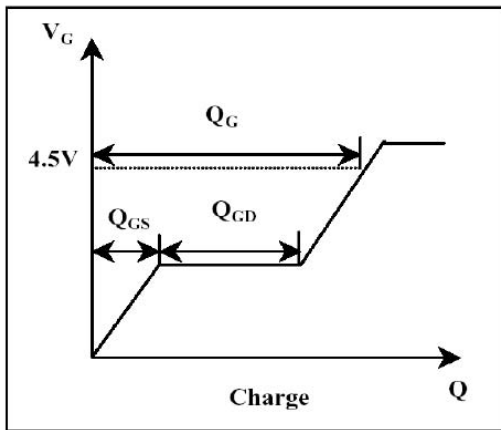


Fig 11. Gate Charge Waveform

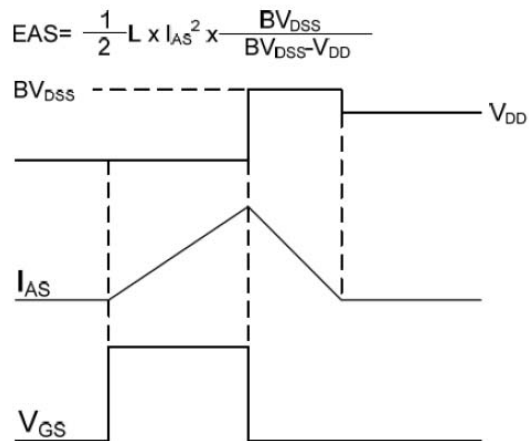


Fig 12. Unclamped Inductive Switching Waveform