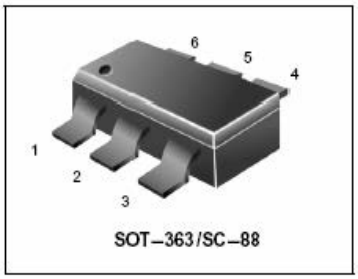
DUAL N-CHANNEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR

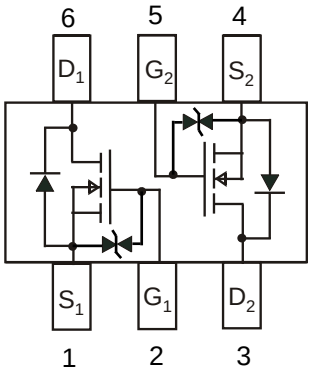
- Low On-Resistance
- Fast Switching Speed
- Low-voltage drive
- Easily designed drive circuits
- Can protect against static electricity 2KV when the product is in use.



DUAL N - Channel - 2KV

Ordering Information(Pb-free)

Device	Marking	Shipping
2N7002EDW	RS	3000 tape/reel



MARKING DIAGRAM & PIN ASSIGNMENT

Maximum Ratings @ T_A=25℃ unless otherwise specified

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	60	V
Gate-Source Voltage	Continuous	V_{GSS}	±20	V
Drain Current	Continuous	I_D	115	mA
	Pulsed	I_{DP} *1	800	mA
Reverse drain current	Continuous	I_{DR}	115	mA
	Pulsed	I_{DRP} *1	800	mA
Total Power Dissipation		Pd *2	225	mW
Channel temperature		Tch	150	℃
Storage Temperature Range		Tstg	-55 to +150	℃

* 1 PW≦10uS, Duty cycle≦1%.
* 2 When mounted on a 1*0.75*0.062 inch glass epoxy board.

DEVICE CHARACTERISTICS

2N7002EDW

Electrical Characteristics @ T_A=25℃ unless otherwise specified, per element

Characteristic	Symbol	Min	Typ	MAX	Unit	Test Condition
OFF CHARACTERISTICS(Note 2)						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	60			V	V_{GS}=0V, I_D=10μA
Zero Gate Voltage Drain Current	I_{DSS}			1.0	μA	V_{DS}=60V, V_{GS}=0V
Gate-source Leakage	I_{GSS}			±10	μA	V_{GS}=±20V, V_{DS}=0V
ON CHARACTERISTICS(Note 2)						
Gate Threshold Voltage	$V_{GS(th)}$	1.0	1.85	2.5	V	V_{DS}=10V, I_D=1mA
Static Drain-Source On-Resistance	$R_{DS(ON)}$			7.5	Ω	V_{GS}=10V, I_D =0.5A
				8.5		V_{GS}=4.5V, I_D=0.2 A
Forward transfer admittance	g_{fs} *	80			mS	V_{DS}=10V, I_D=0.2A
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{iSS}		25	50	pF	V_{DS}=25V
Output Capacitance	C_{OSS}		10	25	pF	V_{GS}=0V
Reverse Transfer Capacitance	C_{rSS}		3.0	5.0	pF	f=1.0MHz
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$T_{D(ON)}$ *		12	20	nS	I_D=0.2A,V_{DD}=30V, V_{GS}=10v,RL=103Ω,RG=6Ω
Turn-On Rise Time	$T_{r(ON)}$ *		14		nS	
Turn-Off Delay Time	$T_{D(OFF)}$*		20	30	nS	
Turn-Off Fall Time	$T_{r(OFF)}$*		22		nS	

* Pw ≦ 300 μs, Duty cycle ≦ 1%

DEVICE CHARACTERISTICS

2N7002EDW

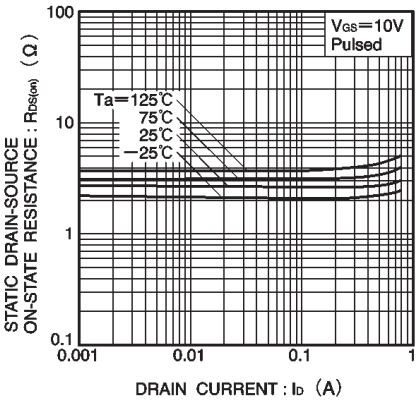


Fig.4 Static drain-source on-state resistance vs. drain current (Ⅰ)

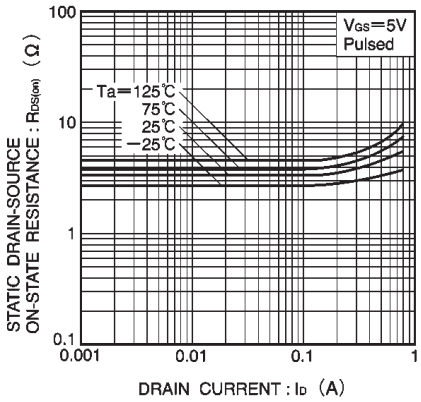


Fig.5 Static drain-source on-state resistance vs. drain current (Ⅱ)

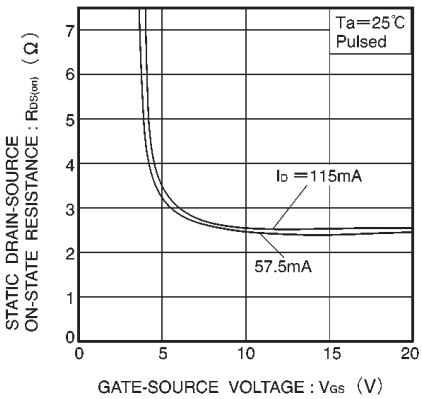


Fig.6 Static drain-source on-state resistance vs. gate-source voltage

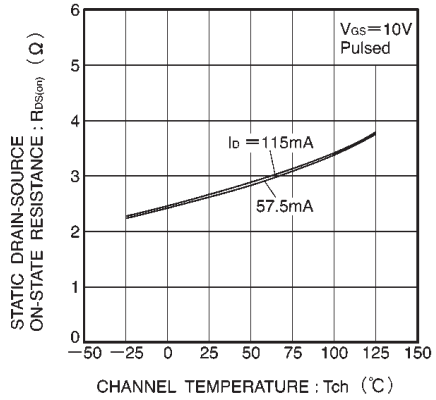


Fig.7 Static drain-source on-state resistance vs. channel temperature

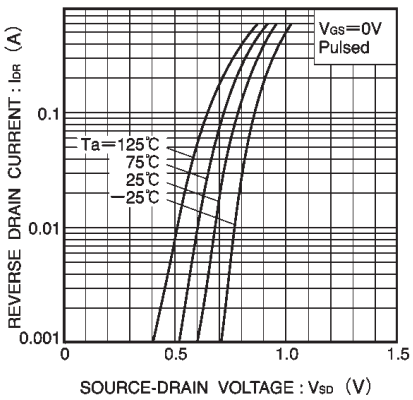


Fig.8 Reverse drain current vs. source-drain voltage (Ⅰ)

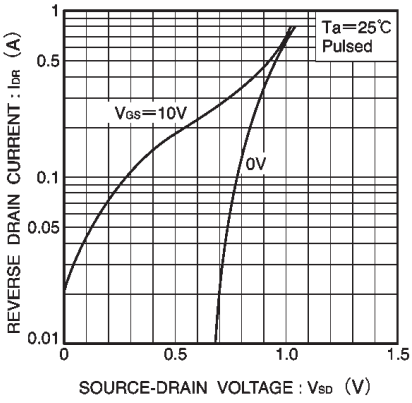


Fig.9 Reverse drain current vs. source-drain voltage (Ⅱ)

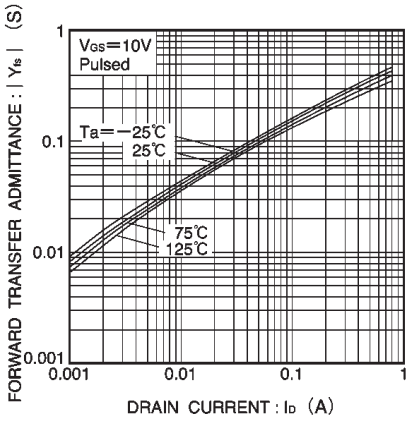


Fig.10 Forward transfer admittance vs. drain current

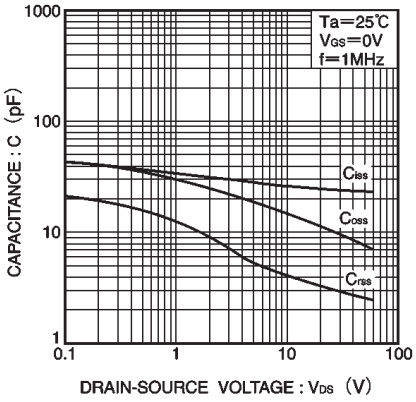


Fig.11 Typical capacitance vs. drain-source voltage

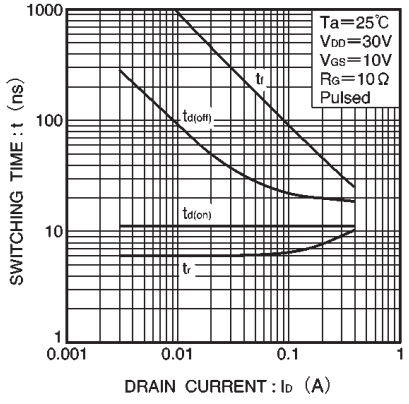
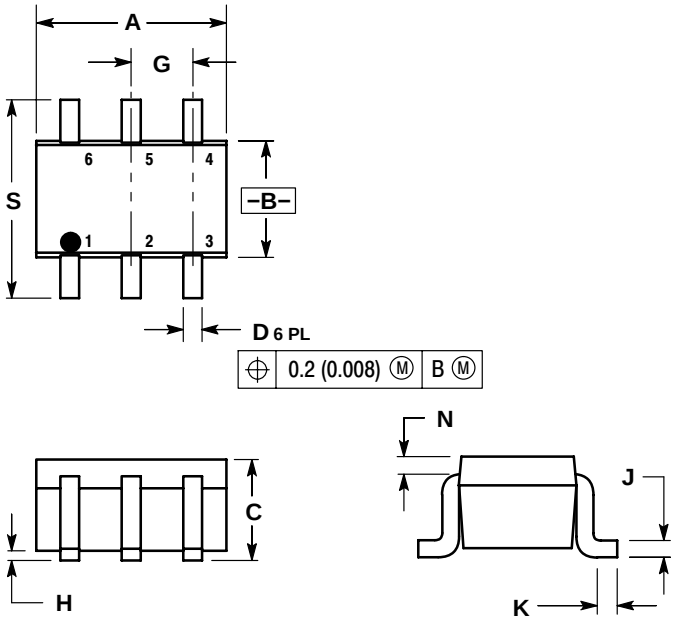


Fig.12 Switching characteristics
(See Figures 13 and 14 for the measurement circuit and resultant waveforms)

PACKAGE OUTLINE & DIMENSIONS

2N7002EDW

SOT-363 (SC-88)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419B−01 OBSOLETE, NEW STANDARD 419B−02.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	−−−	0.004	−−−	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

SOLDERING FOOTPRINT*